UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/463,900	04/03/2000	HANS GUDE GUDESEN	2834-119P	6936

7590 12/18/2002

BIRCH STEWART KOLASCH & BIRCH
P.O. BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER
TRAN, MAI HUONG C

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No.	Applicant(s)
09/463,900	GUDESEN ET AL.
Examiner	**Art Unit**
Mai-Huong Tran	2818

Office Action Summary

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *03 April 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *03 April 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7 & 8*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

The drawings are objected to for the following reasons.

Figure 1 is not designated by a legend such as "Prior Art". The Legend is necessary in order to clarify what applicant's invention is (see MPEP § 608.02g).

Applicant is required to submit a proposed drawing correction, showing changes in red ink, in response to this Office action. However, formal correction of the noted defect(s) can be deferred until the application is allowed by the examiner (see MPEP § 608.02v).

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-16 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,793,115 to Zavracky et al.

Regarding to claim 1, Zavracky discloses a scaleable integrated data processing device, particularly a microcomputer, comprising a processing unit, wherein the

processing unit comprises one or more processors 100, 200, and a storage unit, wherein the storage unit comprises one or more memories 210, 108, and wherein the data processing device is provided on a carrier substrate 220, characterized in that the data processing device comprises mutually adjacent, substantially parallel stacked layers (P, M, MP), that the processing unit and the storage unit are provided in one or more layers, the separate layers being provided with a selected number of processors and memories in selected combinations, that each layer comprises in or on the layer horizontal electrical conducting structures which forms electrical internal connections 114, 224, 140 in the layer, and that each layer comprises further electrical structures which provide electrical connection 140 to other layers and to the exterior of the data processing device as set forth in col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1.

Regarding to claim 2, a scaleable integrated data processing device characterized in that one or more layers are realized in the form of a number of sublayers in a technology which on a first level of a functional hierarchy configures functionally one or more layers as a combined processor and memory layer (MP), or one or more layers substantially as processor layers (P) or one or more layers substantially as memory layers (M) (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 3, a scaleable integrated data processing device, characterized in that the processing unit in a layer (P, MP) is configured functionally on a second level

of the functional hierarchy as one or more processors or parts of one or more processors, at least one processor constituting a central processing unit or microprocessor in the data processing device, and possible further processors optionally being configured as control and/or communication processors respectively (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 4, a scaleable integrated data processing device, characterized in that the central processing unit is configured functionally on a third level of the functional hierarchy as a parallel processor with several execution units working in parallel provided in one and the same layer (P, MP) or in two or more layers (P, MP) or in sublayers of these layers to provide an optimal interconnection topology (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 5, a scaleable integrated data processing device, wherein more than one central processing unit is provided, characterized in that each central processing unit is mutually connected and adapted for working in parallel and provided in one and the same layer (P, MP) or in two or more layers (P, MP) to provide an optimal interconnection topology (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 6, a scaleable integrated data processing device, characterized in that the storage unit in a layer (M, MP) is configured functionally on a second level of

the functional hierarchy as one or more memories or parts of one or more memories at least one memory constituting a RAM and being connected with at least one central processing unit or microprocessor in the data processing device, and possible further memories optionally being configured as high-speed memories, ROMs, WORM, ERASABLE and REWRITEABLE respectively (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 13).

Regarding to claim 7, a scaleable integrated data processing device, characterized in that two or more RAMs are connected to a central processing unit and respectively assigned to two or more subunits in the central processing unit, RAMS and subunits being distributed in selected combinations in one or more layers (P, M, MP) to provide an optimal interconnection topology (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 13).

8. Scaleable integrated data processing device according to claim 6, wherein two or more central processing units which are connected with one or more common RAM or RAMs, characterized in that each central processing unit is provided in mutually adjacent layers (P, MP), or distributed in selected combinations between two or more layers (P, MP), and that the common RAM or RAMs are provided in selected combinations in one or more of the central processing layers (P, MP) and/or in one or more memory layers (M) adjacent to the central processing layers or interfoliated therebetween to provide an optimal interconnection topology (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 13).

Regarding to claim 9, a scaleable integrated data processing device, characterized in that at least a part of the storage unit constitutes a mass memory, the mass memory optionally being configured as RAM, ROM, WORM or ERASABLE or REWRITEABLE or combinations thereof (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 13).

Regarding to claim 10, a scaleable integrated data processing device, wherein the data processing unit comprises several processor layers (P) and several memory layers (M), characterized in that the memory layers (M) in order to reduce the signal paths therebetween and the processor layers (P) are interfoliated between the latter (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 11, a scaleable integrated data processing device, characterized in that further electrical structures in a layer (P, M, MP) are provided on at least a side edge of the layer as an electrical edge connection (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 12, a scaleable integrated data processing device, characterized in that the further electrical conducting structures in a layer (P, M, MP) are provided as vertical conducting structures which form an electrical connection in the cross direction

of the layer and perpendicular to its plane to contact electrical conducting structures in other layers (col. 5, lines 34-67, col. 6, lines 1-63, and fig. 1).

Regarding to claim 13, a scaleable integrated data processing device, characterized in that one or more layers (P, M, MP) are formed of an organic thin-film material, the organic thin-film material or materials being selected among monomers, oligomers and polymeric organic materials and metal organic complexes, or combinations of materials of this kind (cols. 5-15).

Regarding to claim 14, a scaleable integrated data processing device, characterized in that all layers (P, M, MP) are formed of organic thin-film material (cols. 5-15).

Regarding to claim 15, a scaleable integrated data processing device, characterized in that one or more layers (P, M, MP) are formed of inorganic thin-film material, the inorganic thin-film material or materials being selected among crystalline, polycrystalline and amorphous thin-film materials, or combinations of materials of this kind (cols. 5-15).

Regarding to claim 16, a scaleable integrated data processing device characterized in that two or more layers (P, M, MP) are formed of both organic and inorganic thin-film materials or combinations of materials of this kind (cols. 5-15).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran. (703) 305-1958. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (703) 308-4910.

The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mai-Huong Tran

HOAI HO
PRIMARY EXAMINER